

# MP560

## Ka-band GaAs Medium Power Amplifier



- frequency range 26...30 GHz
- small signal gain 17 dB
- output power (P1dB) 28 dBm
- PAE (P1dB) 14%

### Application

- telecommunications
- radars

The MP560 is a Ka-band balanced three-stage medium power amplifier. It has a small signal gain of 17 dB and provides output power of 28 dBm at 1 dB compression point. This MMIC is manufactured using 0.25  $\mu\text{m}$  pHEMT process. The MMIC uses gold bond pads and backside metallization and is fully protected with Silicon Nitride passivation to obtain the highest level of reliability.

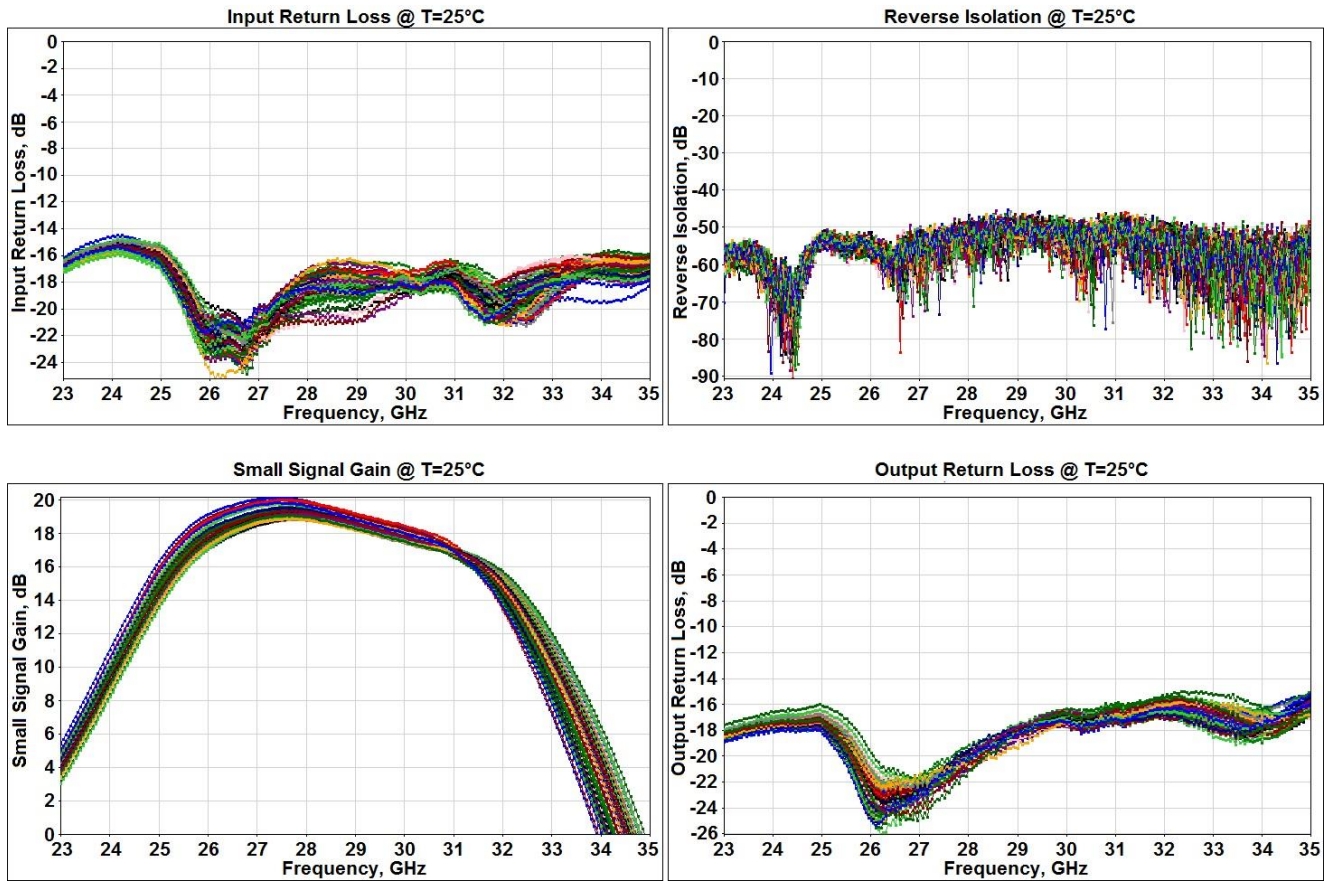
### Electrical Specifications (T = 25 °C)

Symbol	Parameter	Min.	Type	Max.	Unit
$\Delta F$	Frequency range	26	—	30	GHz
S21	Small signal gain	—	17	—	dB
S11	Input return loss	16	—	—	dB
S22	Output return loss	16	—	—	dB
P1dB	Output power for 1 dB compression	28	—	—	dBm
PAE	Power added efficiency at P1dB	—	14	—	%
VD	Supply voltage	—	+6	—	V
VG	Gate bias voltage	-1	—	-0.4	V
I_VD	DC current for supply bus	—	700	—	mA

### Absolute maximum ratings

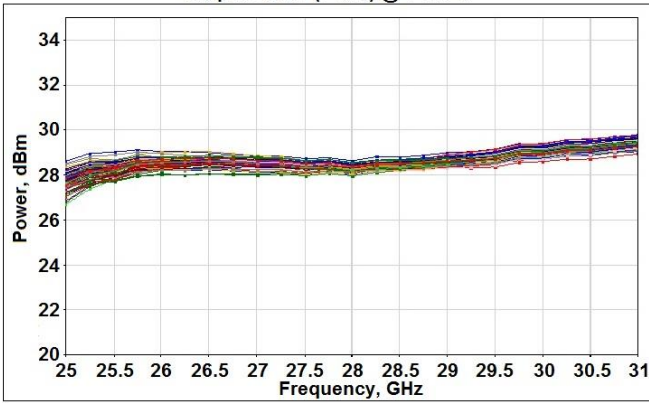
Parameter	Value	Unit
Supply voltage	6	V
Gate bias voltage	-1...-0.4	V
Operating temperature	-40...+85	°C
Storage temperature	-60...+125	°C

Typical characteristics (T = 25 °C)

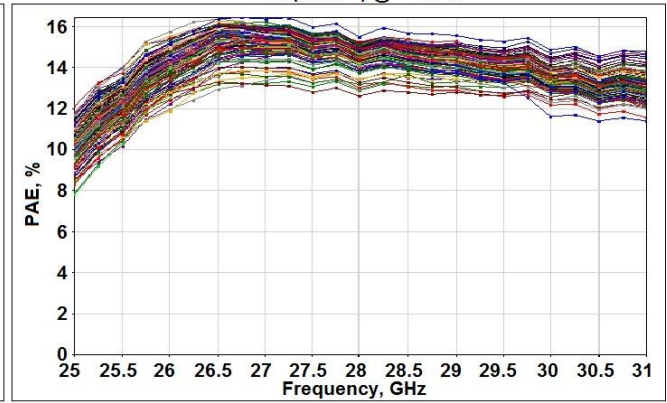


Specifications are subject to change without notice.

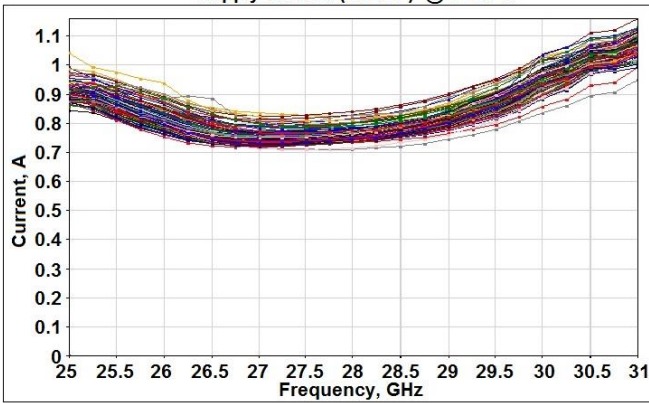
Output Power (P1dB) @ T=25°C



PAE (1dBCP) @ T=25°C

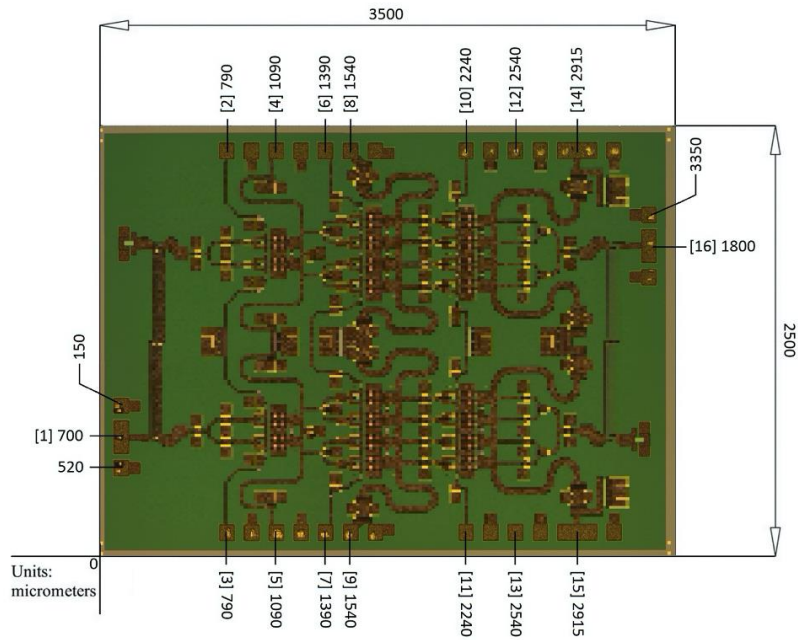


Supply Current (1dBCP) @ T=25°C



Specifications are subject to change without notice.

**Mechanical data**



- Chip size 3500 × 2500 μm (before wafer dicing), thickness 100 μm.
- Position coordinates are shown for the bond pad center.
- Bond pad and backside are metallized with gold.
- RF input, output pads are 200 × 100 μm, DC pads (14 and 15) are 250 × 100 μm, other DC pads are 100 × 100 μm.

Pad number	Pad ID	Voltage, V	Description
1	IN	—	RF Input
2	VG1	-0,4...-1	Gate bias for the first stage of the amplifier
3	VG1	-0,4...-1	Gate bias for the first stage of the amplifier
4	VD1	+6	Drain bias for the first stage of the amplifier
5	VD1	+6	Drain bias for the first stage of the amplifier
6	VG2	-0,4...-1	Gate bias for the second stage of the amplifier
7	VG2	-0,4...-1	Gate bias for the second stage of the amplifier
8	VD2	+6	Drain bias for the second stage of the amplifier
9	VD2	+6	Drain bias for the second stage of the amplifier
10	VG3	-0,4...-1	Gate bias for the third stage of the amplifier
11	VG3	-0,4...-1	Gate bias for the third stage of the amplifier
12	NC	—	Not connected
13	NC	—	Not connected
14	VD3	+6	Drain bias for the third stage of the amplifier
15	VD3	+6	Drain bias for the third stage of the amplifier
16	OUT	—	RF Output

Specifications are subject to change without notice.

**Application notes**

**Mounting**

The chip is back-metallized with gold and can be die mounted with AuSn eutectic alloy or with electrically conductive adhesive. The mounting surface should be clean and flat. The 50 Ohm Microstrip transmission, mounted on 0.127 mm thick alumina and thin film substrates, is recommended for bringing RF to and from the chip (Figure 1). One way to accomplish this is to attach the 0.102 mm thick die to a 0.150 mm thick molybdenum heat spreader (molytab) which is then attached to the ground plane (Figure 2). Microstrip substrates should be located as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.1mm.

**Wire Bonding**

It is recommended for RF pads (1 and 16) to use one wire 25 µm in diameter and 450 µm in length. The recommendation for DC and control pads is one wire 25 µm in diameter and length 700...1000 µm.

**Supply and Bias Arrangement**

The amplifier is activated by setting the gate bias pads (2, 6, 10 and 3, 7, 11) from -0.4 to -1 V, and the drain bias pads (4,8, 14 and 5, 9, 15) to +6 V. Each DC bias pad (VG1, VG2, VG3, VD1, VD2 and VD3) needs to have DC bypass capacitance of 1000 pF as close to the device as possible.

ATTENTION! Make sure the supply voltages are properly sequenced to ensure negative gate bias (VG) is available before applying the positive drain bias (VD).

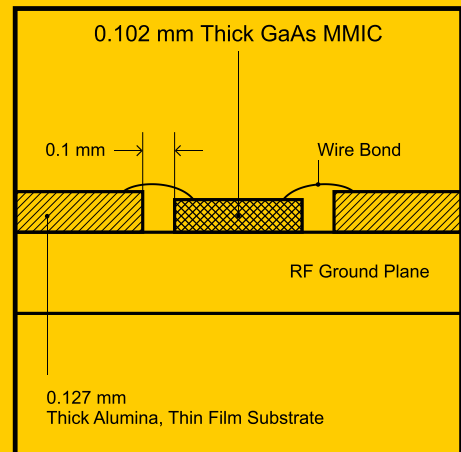


Figure 1.

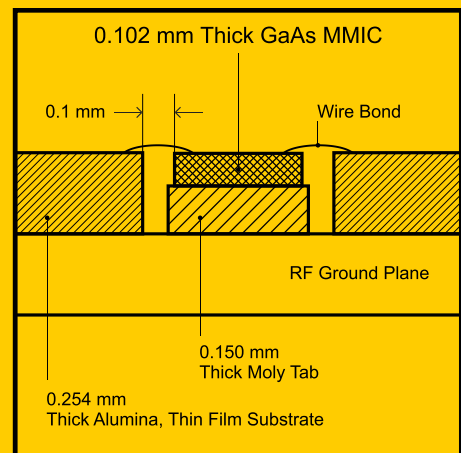


Figure 2.

**Recommended ESD Management**

This device is susceptible to electrostatic and mechanical damage. Dies are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded antistatic workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

